Amendments to the Specification:

Please amend the first paragraph on page 7 as follows:

In a preferred embodiment, the substrate 230 is attached to the conductive cover 270 through a non-adhesive type hermetical seal. For instance, the substrate 230 and the conductive cover 270 can be attached together through an anodic bonding process in a vacuum. Here, the substrate 230 and conductive cover 270 are preferably made of silicon and the cap 250 is preferably made of glass. The outer bonding surface of the cap 250 needs to be planarized and polished. The conductive cover 270 can also be planarized and polished, if needed. The anodic bonding process includes aligning and clamping the substrate 230 and the cap 250, and applying a high voltage between them at a temperature higher than 280C. At an elevated temperature and a high negative potential, the positive ions inside the glass drift away from the glass surface adjacent to the silicon of the conductive cover into the bulk of the glass, and a high electric field is generated across the air gap between the conductive cover 270 and the glass cap 250 due to the depletion of positive ions at the interface. The high electrostatic forces clamp the two bonding surfaces very tightly to form a strong, uniform and hermetic bond.

Please amend the first full paragraph on page 9 as follows:

One step is to planarize and polish either or both surfaces 282, 284 of the glass substrate. This can be done using known techniques. The planarizing removes any fillets on the edges of the vias to support good metallization continuity. The planarizing provides a substantially flat surface to support hermetic sealing as described herein. Moreover, polishing returns transparency to the glass and reduces the possibility of crack propagation by reducing stress points and microcracks. However, planarizing and polishing does not eliminate the rough surface within the vias or recessed cavity, which can contribute to electrical discontinuities, crack propagation, and loss of transparency. Therefore, further steps are needed.

Please amend the first full paragraph on page 11 as follows:

The vias 296 need to be hermetically sealed. One way to provide a hermetic seal for the vias 296 is through the use of conductive covers 270. In one embodiment, the conductive covers 270 are made of silicon and attached to the substrate ~~130~~ 230 in a region opposing the vias 296. The conductive covers 270 are preferably formed from the same silicon wafer that the device microstructure 226 is formed. Moreover, the conductive covers 270 have preferably the same thickness as the device microstructure 226. Making the conductive covers 270 out of the same silicon wafer as the device microstructure 226 reduces the complexity of the manufacturing process. The manufacturing of silicon devices is known in the art and is not covered here. An alternative process to hermetically seal the vias 296 is to use a solder ball. The process steps include placing the solder ball onto the via 296, performing solder ball degassing, and melting the ball in vacuum to hermetically seal 297 the via 296.